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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,837	10/31/2003	Cynthia H. Polsky	109263-132220	1277

31817 7590 02/11/2008  
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EXAMINER
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ROSE, KIESHA L

ART UNIT	PAPER NUMBER
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2822

MAIL DATE	DELIVERY MODE
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02/11/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/698,837

**Applicant(s)**

POLSKY ET AL.

**Examiner**

Kiesha L. Rose

**Art Unit**

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 4/17/07.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 6-9, 11, 12 and 26-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-9, 11, 12 and 26-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB06)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

This Office Action is in response to the amendment filed 4/17/07.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31-32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 31-32 is considered new matter because the limitation, the 2nd microelectronic die has an interconnect layer on the first and second side of the 2nd die and a via extending from the first and second side to couple the two interconnects together and in regards to claim 32, the limitation of a redistributed interconnect of the interconnect of the 2<sup>nd</sup> die is coupled to the interconnect.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 31 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 31 discloses **the interconnect** being disposed on a selected side. It is unclear what interconnect is being referred to. For examining purposes, the interconnect is going to be referred to as the interconnect of the second microelectronic die.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6-9, 26-27 and 30-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Higgins (U.S. Patent 6,064,114).

In re claims 1 and 26, Higgins discloses a semiconductor device (Figs. 1 and 2) that contains a carrier substrate (PCB, column 3, lines 42-48) with bond pads, a microelectronic die (60) having an active (bottom of 60) and backside (top of 60) with an active side interconnect (56) disposed on the active side and coupled to the bond pad of the carrier substrate, a backside interconnect (top of layer 54 on the backside of the die) disposed on the backside, coupled to and in substantial vertical alignment with the active side interconnect, a redistributed interconnect (52) of the backside interconnect disposed on the backside, coupled to and offset from the backside interconnect, an

interconnect material (20) comprising a conductive material without a wire stem (electrically reflowable material, (cl 26)) (solder) (20) being coupled directly to the redistributed interconnect and an interconnect (16) of the second microelectronic die substrate (11) electrically and directly coupled to the interconnect material.

In re claim 7, the first die comprises a metal layer (56) having a first side and a second side, a first dielectric layer (57) adjacent to the first side of the metal layer, a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect, a second dielectric layer (57) adjacent to the second side of the metal layer and a via (54) extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

In re claim 8, the redistributed interconnect comprises a conductive trace (52) coupled to and extending from the backside interconnect to a selected location and a third dielectric layer (53) overlaying the conductive trace and an aperture in the third dielectric layer at the selected location.

In re claim 9, the selected location for the redistributed interconnect corresponds to the interconnect of the second microelectronic die. (Fig. 2)

In re claim 12, the redistributed interconnect is not in vertically alignment with the backside interconnect. (Fig. 2)

In re claim 27, the electrically conductive reflowable material is lead solder or lead-free solder. (Column 2, line 40)

In re claim 30, the second microelectronic die comprises an active side (area where 20 is) and a backside (area where 10 is), and wherein the interconnect is disposed on the active side of the second microelectronic die.

In re claim 31, the second microelectronic die has first side (area where 20 is) and a second side (opposite side of area where 20 is), the interconnect (15/16) being disposed on the first side and another interconnect being disposed on the second side and a via extending from the first side to the second side to electrically couple the interconnect to the other interconnect. (Col. 2, lines 26-35)

In re claim 32, the second microelectronic die includes a redistributed interconnect of the interconnect of the first side and is coupled to and offset from the other interconnect. (Col. 2, lines 26-35) Higgins discloses that the 2nd die has multiple interconnect layers that are stacked on top of each other. Those skilled in the art would know that there would vias between the multiple layers to form an electrical connection between the two.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins.

In re claim 11, Higgins discloses all the limitations except for the second substrate being coupled to the redistributed interconnect by a process of reflow bonding, thermal compression or ultrasonic bonding, a "*product by process*" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "*product by, all of*" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear. Even though product –by [-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted)."

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins in view of Schueller et al. (U.S. Patent 5,844,168).

In re claim 28, Higgins discloses a semiconductor device (Figs. 1 and 2) that contains a carrier substrate (PCB, column 3, lines 42-48) with bond pads, a

microelectronic die (60) having an active (bottom of 60) and back side (top of 60) with an active side interconnect (56) disposed on the active side, a backside interconnect (54) disposed on the backside, coupled to and in substantial vertical alignment with the active side interconnect, a redistributed interconnect (52) of the backside interconnect disposed on the backside, coupled to and offset from the backside interconnect, an interconnect material (20) comprising a conductive material (20) being coupled directly to the redistributed interconnect and an interconnect (16) of the second microelectronic die substrate (11) electrically and directly coupled to the interconnect material. Higgins discloses all the limitations except for the interconnect material to be an electrically conductive adhesive. Whereas Schueller discloses an interconnect structure (Fig. 3) that contains a conductive material (360/340) that contains an electrically conductive adhesive or a solder material. The interconnect material is formed of an electrically conductive adhesive for electrical connection to a other layers (PCB). (column 7, lines 34-44) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Higgins by incorporating the interconnect layer to be an electrically conductive adhesive to allow for electrical connection to other layers (PCB) as taught by Schueller.

In re claim 29, Schueller discloses the interconnect material is silver loaded epoxy. (Column 7, lines 35-38)

### ***Response to Arguments***

Applicant's arguments filed 4/17/07 have been fully considered but they are not persuasive. Applicant argues that the Higgins reference does not include a backside interconnect. As shown the backside interconnect is the top of the via (54), which produces an electrical interconnect on the backside of the die. Applicant also argues that the die is a substrate not a die, this is erroneous as the layer (60) is a die and can also function as a substrate and layer 60 has an active layer. Higgins discloses that there is no redistributed interconnect layer on the backside interconnect, this is erroneous as seen in Fig. 1/2, the backside interconnect is the top of layer 54 and the redistributed interconnect is layer 52 which is connected and offset from the backside interconnect as claimed. Lastly, Applicant's argue that the interconnect of the 2<sup>nd</sup> die is not coupled to the redistributed layer, as shown in Figs. 1/2 and Col. 2, line 20, the interconnect layer( 15/16) of the 2<sup>nd</sup> die is coupled to the redistributed layer through the interconnect material (20). As shown the Higgins reference discloses the claimed limitations and the rejections stand.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

/Kiesha L. Rose/

Primary Examiner, Art Unit 2822